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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,298	12/31/2003	Peter Hazucha	INTEL-0057	8425

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,298	HAZUCHA ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-27* is/are allowed.

6)☒ Claim(s) *1-4,6,7,12-15,17,18,21-23 and 28-30* is/are rejected.

7)☒ Claim(s) *5,8-11,16 and 19-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-30 are presented in the instant application according to the Applicants' filing on 12/31/2003.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 21-23 and 28-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 21, the recitation "a switch; a converter; a timing circuit to control input of a voltage signal" appears to be mis-descriptive since, according to page 11, lines 11-12, in the specification of the claimed invention, the converter includes the timing circuit [100] and the switch [110, 120], in other words the converter is not a separate item from the timing circuit

and the switch, as such the claimed language is required to be consistent with the disclosure in the specification. Clarification is required.

Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: a first circuit and a second circuit. Clarification is required.

Claims 22-23 and 29-30 are also rejected under 35 U.S.C. 112, second paragraph because of their dependency on claim 21 and claim 28, respectively.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-7, 12-15, 17-18 and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Eitrheim (U.S. Patent No. 5,638,016).

With respect to claims 1 and 12, Eitrheim discloses, in Figs. 1 and 7, a circuit and its corresponding method, the circuit comprising a first delay line [Δ1] to delay a clock signal [Input Clock] by a first amount of time [Δ1]; a second delay line [Δ2] to delay the clock signal by a second amount of time [Δ1]; and a signal processor [28] to generate a timing signal [Φ1] from the clock signal, the timing signal having a first edge controlled by the delayed clock signal generated by the first delay line and a second edge controlled by the delayed clock signal generated by the second delay line *(Fig. 7)*.

With respect to claims 2 and 13, Eitrheim discloses, in Fig. 7, that the timing signal assumes different logical values over a predetermined time period.

With respect to claims 3 and 14, Eitrheim discloses, in Fig. 7, that the timing signal assumes a first logical value for a longer duration than a second logical value over the time period.

With respect to claims 4 and 15, Eitrheim discloses, in Figs. 1 and 7, a control circuit [24, 26] to generate an interim timing signal from the clock signal, the interim timing signal having edge transitions which coincide with one of a falling edge and a rising edge of the clock signal; and a timing circuit to generate the timing signal from the interim timing signal.

With respect to claims 6 and 17, Eitrheim discloses, in Fig. 7, that the timing circuit sets the first edge of the timing signal based on an edge transition of the delayed clock signal generated by the first delay line, and sets the second edge of the timing signal based on an edge transition of the delayed clock signal generated by the second delay line.

With respect to claims 7 and 18, Eitrheim discloses, in Fig. 7, that the first edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the delayed clock signal generated by the first delay line, and wherein the second edge of the timing signal corresponds to a logical value of the interim timing signal that exists at the time of the edge transition of the delayed clock signal generated by the second delay line.

With respect to claims 28 and 30, as best understood, Eitrheim discloses, in Figs. 1 and 7, a system comprising a first circuit [memory, RAM, col. 1, line 52], and a second circuit [Fig. 1] comprising (a) a first delay line [Δ1] to delay a clock signal by a first amount of time [Δ1]; (b) a

second delay line [Δ2] to delay the clock signal by a second amount of time [Δ2]; and (c) a signal processor [28] to generate a timing signal [Φ1] from the clock signal, the timing signal having a first edge controlled by the delayed clock signal generated by the first delay line and a second edge controlled by the delayed clock signal generated by the second delay line, wherein the timing signal controls operation of the first circuit.

With respect to claim 29, Eitrheim discloses, in Figs. 1 and 7, that the timing signal assumes different logical values over a predetermined time period, and wherein each logical value controls a different function of the first circuit.

Allowable Subject Matter

5. Claims 24-27 are allowed.

6. Claims 5, 8-11, 16 and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 21-23 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this office action.

8. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A circuit, in which the interim timing signal has a period which is substantially twice as long as the period of the clock signal, as called for in claims 5 and 16;

b) A circuit including a first logical transfer circuit to store logical values of the interim timing signal prior to respective edge transitions of the delayed clock signals generated by the

first and second delay lines, the first logical transfer circuit introducing delay that contributes to setting of the first and second edges of the timing signal, as called for in claims 8 and 19;

c) A method including a step of changing at least one of the first and second amounts of delay to adjust a position of at least a corresponding one of the first and second edges of the timing signal, as called for in claim 20;

d) A circuit, in which a controller to change at least one of the first and second amounts of time in the delay lines to adjust a position of at least a corresponding one of the first and second edges of the timing signal, as called for in claim 11;

e) A circuit, in which a timing circuit to control input of a voltage signal into a converter through a switch, a signal processor to generate a timing signal and different portions of the timing signal independently control switching of the voltage signal into the converter, as called for in independent claim 21; and

f) A method including a step of controlling input of a voltage signal into a level converter based on a timing signal, in which different portions of the timing signal independently control switching of the voltage signal into the level converter, as called for in independent claim 24;

Citation of Relevant Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Otsuka (U.S. Pub. No. 2002/0083358) discloses generation of pulse signals from a clock signal.

Prior art McClure (U.S. Patent No. 6,603,338) discloses a device and method for address input buffering.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER